



## A Multiple DSP System for Speech Processing Applications

C. G. Rowden and C. F. Chan

The design of a novel and cost-effective parallel processing system using digital signal processors (DSPs) is presented. The system can accommodate up to 16 TMS32010 processors with a total processing power of 80 MIPS. Its main application areas are speech analysis/synthesis and low bit-rate coding of speech signal for telecommunication purposes. The system can be classified as a MIMD machine. Each processor on the system has its own local memory for program and data storage. The system utilizes a dedicated local bus for processor-to-processor communications with a loosely-coupled scheduling policy. By using a simple and flexible message switch for routing the data traffic between processors, the system can emulate a wide variety of connection topologies, including pipelining and perfect shuffle network.

A prototype has been built in which each processing element occupies one S-100 card and memory has shared access with a host computer running a general purpose operating system. This arrangement is very convenient for downloading programs and monitoring execution during system development. An example of implementing a 9 kbit/s multipulse speech coder on this parallel processing system will be given.

Department of Electronic Systems Engineering, University of  
Essex, UK